ADQ35-PDRX Datasheet

The ADQ35-PDRX is a high-speed digitizer with extended dynamic range for pulse data applications. The ADQ35-PDRX features:

- **One analog input channel**
- **12 bits resolution**
- **3.5 bits dynamic range extension through built-in dual-gain channel combination**
- **5 GSPS sampling rate**
- **14 Gbyte/s sustained data transfer rate to GPU**
- **14 Gbyte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**
- **Continuous streaming to GPU**

1 ORDERING INFORMATION

ADQ35-PDRX is available with a set of options listed in Table 1. Selection is done in three steps:

1. Select analog front-end configuration among related products.
2. Select the firmware options. The firmware FWDAQ is always included. Additional firmware options can be loaded into the board at any time.
3. Add additional features.

Table 1 Ordering information

Order code	Description	Datasheet	User guide
Related products: Hardware analog front-end options[1]			
ADQ35-PDRX	Built-in dual-gain front-end. This document	**22-2919**	21-2539
ADQ35	General purpose DC-coupled front-end	22-2918	21-2539
ADQ35-WB	AC-coupled wideband front-end for RF systems	20-2509	21-2539
Firmware options			
-FWDAQ	Included data acquisition firmware. This document.	**22-2919**	21-2539
-FWATD	Firmware advanced time domain. Add thresholding and waveform averaging in FPGA	22-2912	21-2539
-FWPD	Firmware pulse detection. Detect and analyze pulses in FPGA.	23-3028	21-2539
Additional features			
DEVDAQ[2]	Open FPGA for **FWDAQ**		20-2507
-W5Y	Extended warranty 5 years		

[1] The hardware options are factory installed and cannot be retrofit.

[2] The development kit **DEVDAQ** opens the FPGA for the user to add custom functions. **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project using **DEVDAQ** can be used on any ADQ35-PDRX with a valid **FWDAQ** license.

2 ADQ35-PDRX INTRODUCTION

2.1 Features

- One input channel
- 5 GSPS sampling rate
- 12 bits resolution
- 3 bits dynamic range extension through built-in dual gain channel combination
- DC-coupled with 2 GHz bandwidth
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbytes data memory
- 14 Gbyte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x16
- Averaging firmware FWATD
- Pulse analysis firmware FWPD
- Open FPGA enables custom firmware

2.2 Applications

- Time-of-flight mass spectrometry
- LIDAR
- Pulse data systems

2.3 Advantages

- ADQ35-PDRX integrates the analog dual-gain amplifier for a compact high-performance system solution
- Real-time processing for pulse data capture and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ35-PDRX uses a built-in dual-gain channel combination to increase the dynamic range in pulse capture. Weak pulses are captured through a channel with high gain and strong pulses are captured through a channel with low gain. The channel combination results in a dynamic range extension equivalent to 3 extra bits of vertical resolution.

The PDRX channel combination is carried out by the digitizer firmware and is available for **FWATD**, **FWPD** and **FWDAQ**.

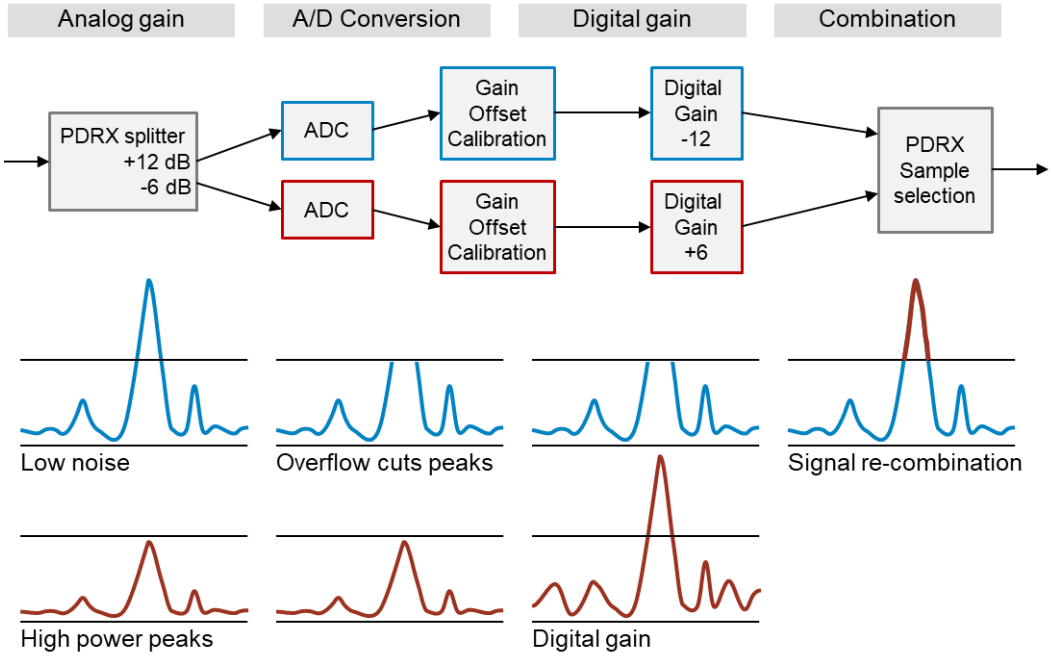

Figure 1 Principle of channel combination.

The ADQ35-PDRX hardware can also be used for custom channel combination. The combination firmware is then bypassed, and the board operate with 2 channels output.

In addition to the specific pulse detection, ADQ35-PDRX supports a variety of options for efficient system design:

Streaming to GPU
ADQ35-PDRX supports up to 14 Gbyte/s sustained peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms. Note that streaming of all data is possible, which enables dead-time free recording.

Streaming to CPU
ADQ35-PDRX supports up to 14 Gbyte/s sustained streaming to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ35-PDRX offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

3 TECHNICAL DATA

Technical parameters are valid for ADQ35-PDRX operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 2 Analog input (front panel label A)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels			1		
Sampling rate			5		Gsample/s
Bandwidth	-3dB		2		GHz
Input range			1.1		Vpp
Input impedance			50		Ω
Coupling		DC			
Connector type		SMA			
Programmable DC-offset					
DC-offset range		-0.5		+0.5	V
Dynamic performance					
Idle channel noise[3]			68		dBFS
ENOB noise based[4]			11.0		bits

Table 3 Comparison of ADQ35-PDRX to ADQ35

Parameter	Condition	ADQ35	ADQ35-PDRX	Unit
RMS noise	Terminated input	394	140	µV
Max input range		0.5	1.1	Vpp
DC-offset		-0.25 to 0.25	-0.5 to 0.5	V
Dynamic range[5]		53	68	dB
ENOB[6]		8.5	11.1	bits
Bandwidth	-3dBFS	2.5	2	GHz
Dual-gain gain ratio		-	11.3 (21 dB)	

[3] Measured integrated noise with a terminated input. Noise level is computed relative a full-scale sine wave.
[4] Computed from idle channel noise. See figure for ENOB at sweep of input power.
[5] Power of full-scale sine wave relative noise with terminated input.
[6] Computed from “Dynamic Range” in

Table 3 using the formula (Dynamic Range – 1.76) / 6.02.

Table 4 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator [7]					
Frequency range 1			5000	5050[8]	MHz
Frequency range 2			4000		MHz
Frequency range 3			3000		MHz
External clock reference input (from front panel CLK connector) [9] [10]					
Frequency		1	10	500	MHz
Frequency [11]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [12]	AC		200		Ω
Connector type		SMA			
Clock reference output (on front panel CLK connector)[13]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω

[7] The internal clock generator can generate frequencies in three different ranges.
[8] If the external clock reference deviates from its nominal value, the clock frequency can differ from expected. This is the maximum value where operation can be maintained.
[9] Clock reference from an external source to synchronize the ADQ35-PDRX to the external source.
[10] To minimize sampling clock jitter, the external reference should have as steep edges as possible. Therefore, a square wave with sharp edges is preferred over a sinewave, particularly at lower reference frequencies and amplitudes.
[11] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[12] Software-selectable high-impedance mode.
[13] The internal clock reference of the ADQ35-PDRX is made available to synchronize external equipment.

Table 5 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [14]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [15]	As trigger		50		ps
Update rate [15]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 6 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [14]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [15]	As trigger		3.2		ns
Update rate [15]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[14] Software-selectable high-impedance mode, suitable for source terminated signals.

[15] Timing properties are valid for 5 GSPS. Timing properties scale linearly with sampling frequency.

Table 7 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input					
Impedance			50		Ω
Impedance (high) [16]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [17]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [17]				156.25	MHz

Table 8 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [18]	FWDAQ		48		W
Power supply		10.8	12	13.2	V
Operating temperature	FWDAQ[19]	0		55	°C
Operating temperature	FW options[20]	0		45	°C
Size					
Width			18.42		mm
Length			269.55		mm
Height			111.15		mm
Weight			600		g
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[16] Software-selectable high-impedance mode, suitable for source terminated signals.
[17] Timing properties are valid for 5 GSPS. Timing properties scale linearly with sampling frequency.
[18] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 10 Gbyte/s to PC.
[19] Operating the ADQ35-PDRX with FWDAQ and streaming data up to 10 Gbyte/s.
[20] Using firmware options from Teledyne SP Devices. Custom firmware designs may result in higher power consumption and thereby lower temperature range.

Table 9 Custom GPIO expansion. See section 10.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential input signals LVDS[21]	8
Number of single-ended 3.3-V LVCMOS I/O signals	5
Control bus	I2C, 3.3 V
Power supply	1.8 V, max 300 mA 3.3 V, max 1 A 5 V, max 600 mA

Table 10 Software support

Parameter	Value
Operating system[22]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++
High-level API	LabVIEW / MATLAB / C#

Table 11 Data transfer[23]

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes[24] [25]	1 / 4 / 8 /16	
Sustained data rate to CPU / GPU	14	Gbyte/s
Sustained data rate peer-to-peer to GPU	14	Gbyte/s
Data format to CPU [26]	32 / 16 / 8	bits
Data format for streaming to GPU	32 / 16 / 12 / 10 / 8	bits

[21] The port can be set to output through the open FPGA development kit DEVDAQ.
[22] See 15-1494 Operating system support for a detailed listing of supported distributions.
[23] This is the data rate that the ADQ35-PDRX supports. Other parts of the system may limit the performance.
[24] The ADQ35-PDRX must be installed in a 16 lanes slot or a slot with a connector with an open end. If a shorter connector is used, the number of lanes and the maximum data rate is limited.
[25] Bifurcation required for 16 lanes.
[26] Default 16 bits MSB-aligned.

Table 12 Data acquisition

Parameter	Condition / Description	Min	Typical	Max	Unit
Rearm time[27]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	2-channel mode in steps of 1	2		2^{32}-1	samples
	Combined channels	2		2^{32}-1	samples
Pre-trigger[28]	2 channels mode in steps of 16	0		16 336	samples
	Combined in steps of 16	0		16 336	samples
Trigger delay[29]	2 channels mode in steps of 16	0		2^{36}-16	samples
	Combined in steps of 16	0		2^{36}-16	samples
Trigger sources[30]	Start recording a set of data	External “TRIG”, “SYNC” and “GPIO” Logic OR of external sources Channel Logic OR of channels Internal generators Software			
Recording modes	Record length setting	Static (set by user) Dynamic (data controlled) Gated (trigger controlled) Continuous (unlimited)			
Timestamp reset	Reset or synchronize timestamp	External “TRIG”, “SYNC” and “GPIO” Software Internal periodic pulse generator			

[27] Minimum time from the last sample of a record to the next trigger.
[28] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[29] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[30] Trigger sources can be synchronized to clock reference for synchronous systems

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

Table 13 Digital signal processing blocks

Object	Description
Digital Baseline Stabilizer (DBS)	Track and adjust the baseline to target level
Digital gain	Digital scaling of the signal
Digital offset	Add digital offset to signal
Digital FIR filter	User controlled 17 tap FIR filter
Sample skip	Skip samples after filtering to adjust sampling rate

Table 14 Pattern generators

Object	Description
Pattern generator	2 instances of general pattern generators
Periodic pulse generator	4 instances of periodic pulse generator

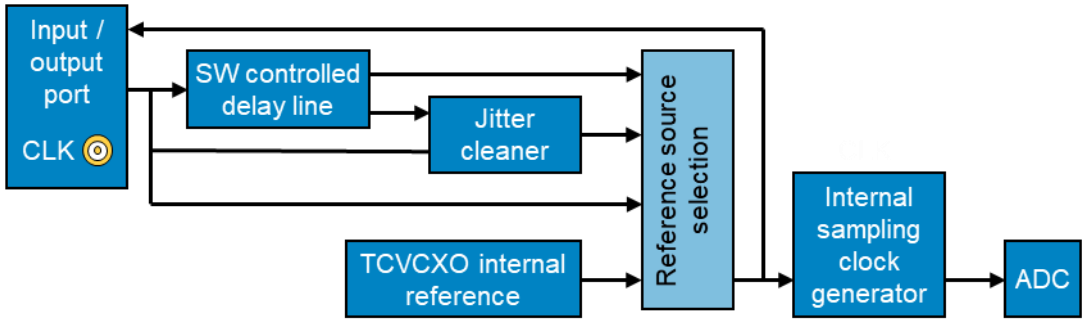

Figure 2 Clock generation block diagram.

Table 15 Clock generation

Function	Modes
Clock reference Phase and frequency reference for the clock system	Internal External through SMA connector CLK External with jitter cleaner and/or delay line
Sampling clock ADC sampling clock	Internal clock generator
Clock reference output	Internal clock reference (if selected as source)

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

The channel combination is included in FWDAQ for ADQ35-PDRX hardware.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

The channel combination is included in FWATD for ADQ35-PDRX hardware.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

The channel combination is included in FWPD for ADQ35-PDRX hardware.

5.4 Managing firmware

The ADQ35-PDRX includes methods for managing different firmware options:

- The non-volatile memory on the digitizer can store up to four different firmware images, including the active firmware. The tool ADQAssist is used to change active image and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware images.
- If all firmware images of interest cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer and the host computer must be power cycled to complete the switch of firmware image. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section **Error! Reference source not found.** for details about available firmware features.

6 ABSLOUTE MAXIMUM RATINGS

Table 16 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature[31]		0	55	°C
Storage temperature		-40	70	°C
Analog in	Peak	-7	+7	V
	DC	-3	+3	V
TRIG, SYNC in 50-Ω mode	Powered	-2	5	V
	Not powered	-2	2	V
TRIG, SYNC in 500-Ω mode	Powered	-2	6	V
	Not powered	-2	2	V
CLK REF	AC		5	Vpp
	DC	-5	5	V
GPIO	Powered	-1.5	5	V
	Not powered	-1.5	1.5	V
FFC / FPC differential signal to GND	Powered[32]	-0.5	2.3	V
	Not powered[32]	-0.5	0.5	V
FFC / FPC single-ended signal to GND	Powered[32]	-0.3	3.8	V
	Not powered[32]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[31] The absolute maximum temperature is the range where it is allowed to start the board.

[32] The absolute maximum ratings depend on whether the ADQ35-PDRX is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

7 TYPICAL PERFORMANCE

7.1 Time domain pulse data

Pulse examples of different amplitude are plotted showing a ratio of 500 : 1. The pulses are compared with ADQ35 for reference to illustrate the benefit of ADQ35-PDRX in this application. Notice that other applications may benefit from the properties of ADQ35 instead.

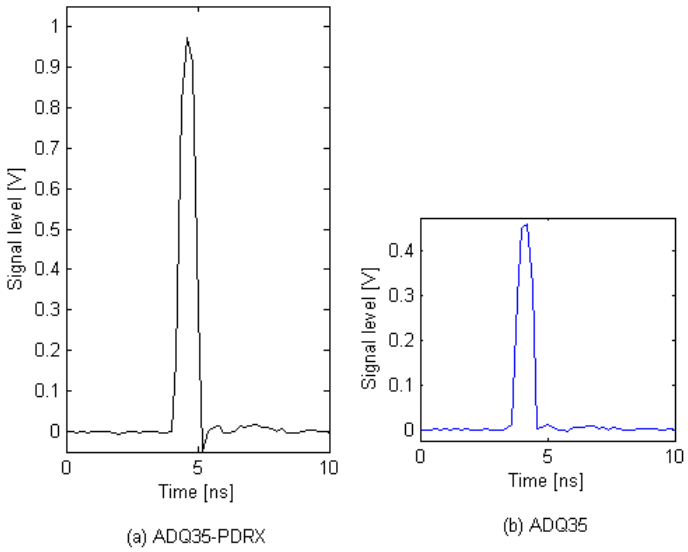

Figure 3 Time domain plot of pulses at 90% of full-scale for the respective digitizer. Notice that ADQ35-PDRX can accept larger signals without overrange.

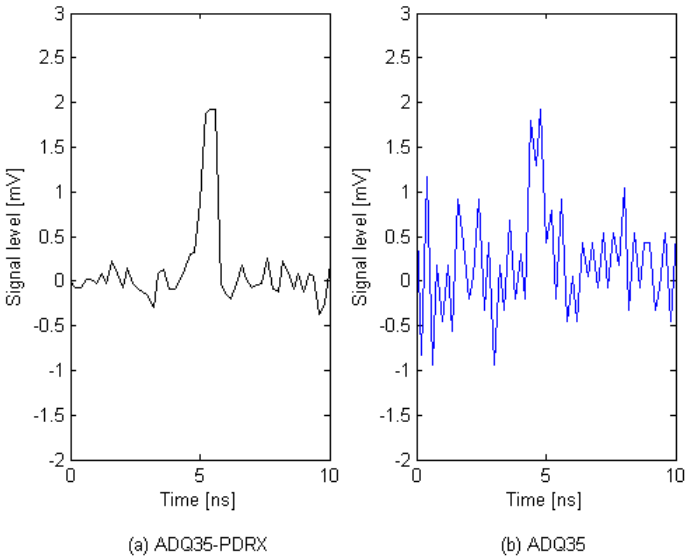

Figure 4 Time domain plot pulse at 2 mV. Notice that the pulse is easier to detect in the ADQ35-PDRX which has lower noise than the ADQ35.

7.2 Time domain pulse accuracy

Pulse amplitude accuracy for the combined signal is measured in amplitude sweep.

This is a measurement of the static gain. The amplitude measurement of a wide pulse is related to the input signal amplitude. The deviation from the expected value in percent relative signal level and relative full scale is shown.

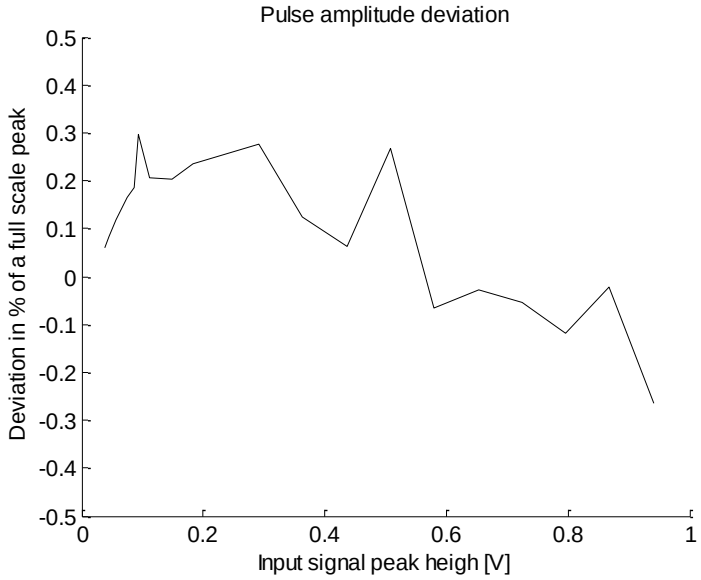

Figure 5 Deviation from ideal pulse height relative to full-scale pulse.

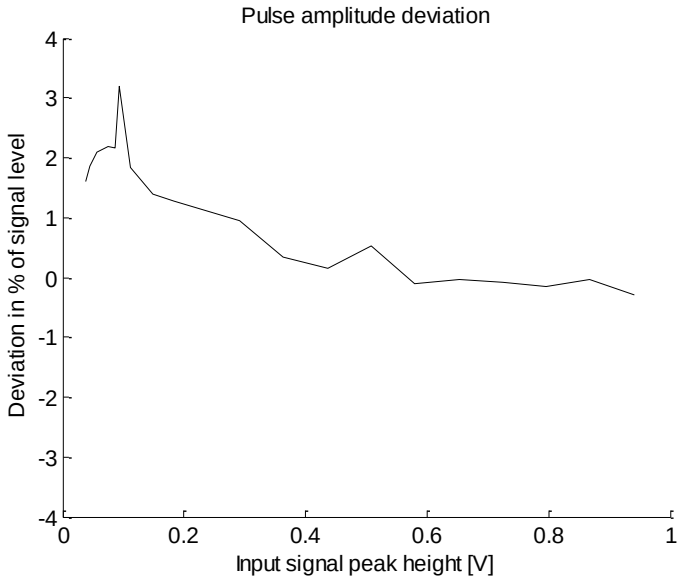

Figure 6 Deviation from ideal pulse height relative pulse level.

7.3 Timing accuracy

The timing between the Low gain and the High gain channels is measured over frequency to verify that pulse timing is preserved.

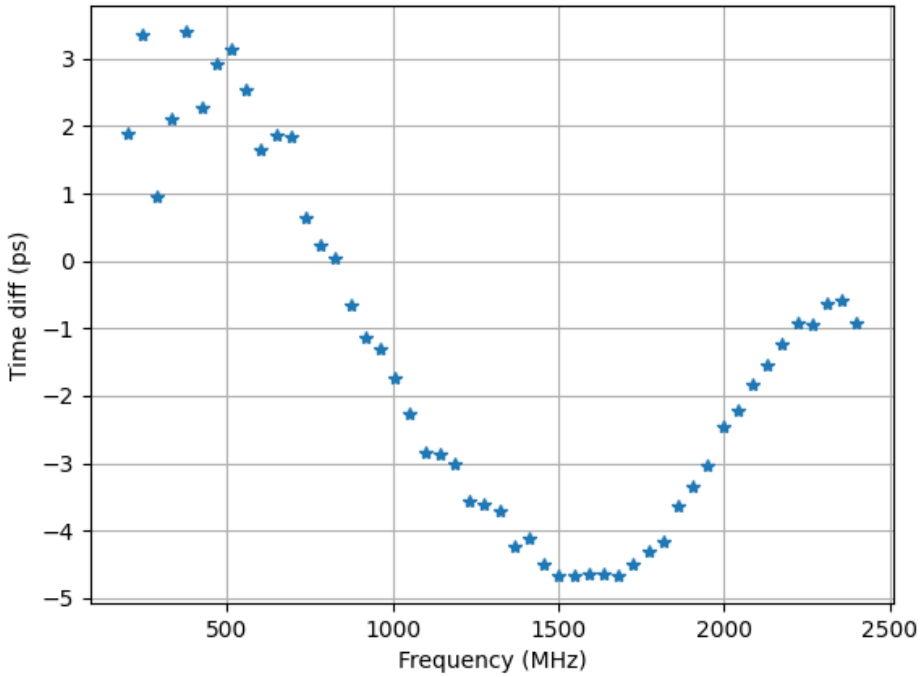

Figure 7 Timing difference between high gain and low gain channels.

7.4 Frequency response

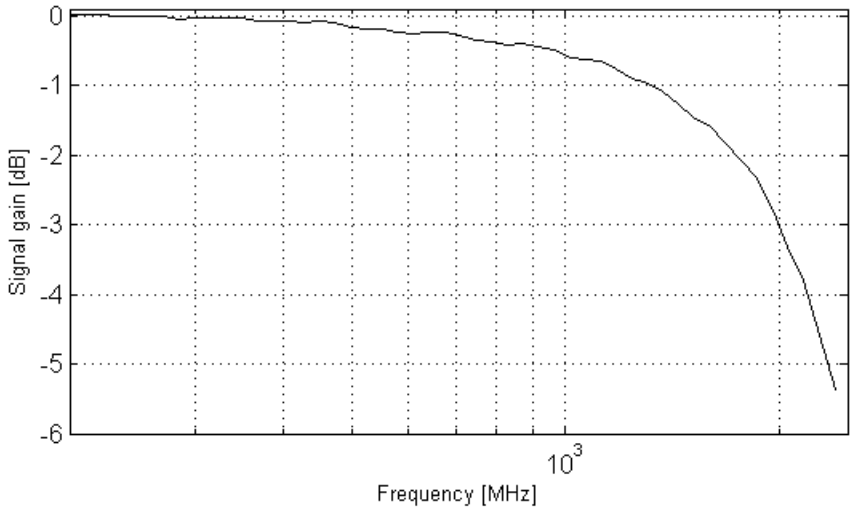

Figure 8 Frequency response, typical performance.

8 BLOCK DIAGRAM

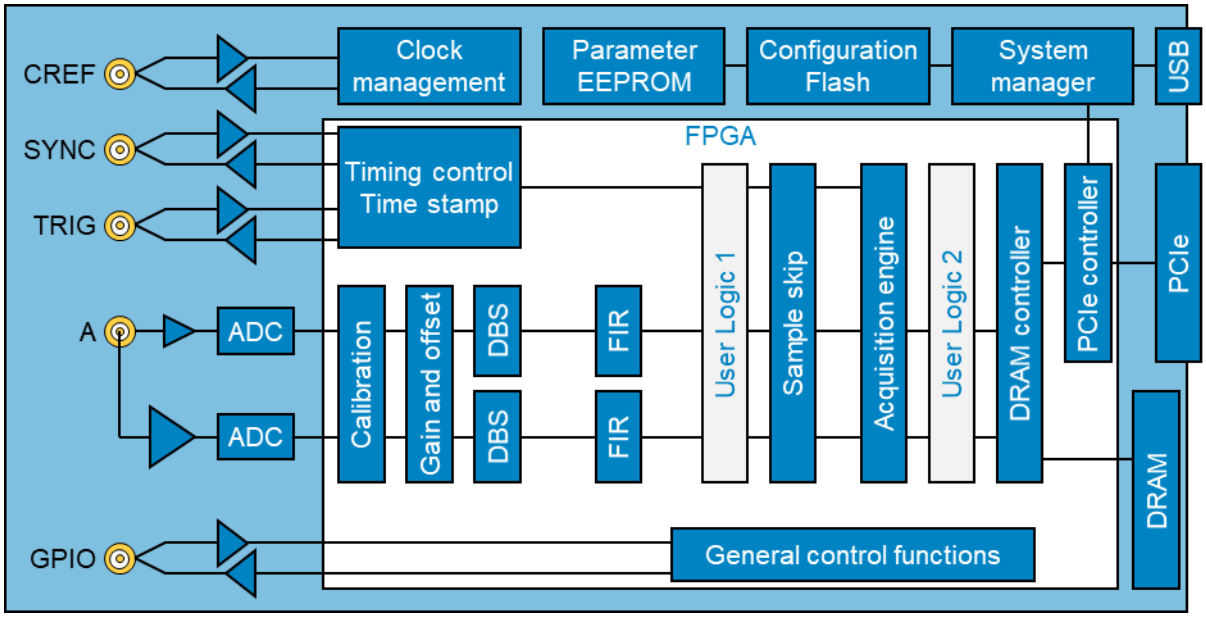

Figure 9 Block diagram ADQ35-PDRX-FWDAQ-PCIe bypass channel combination

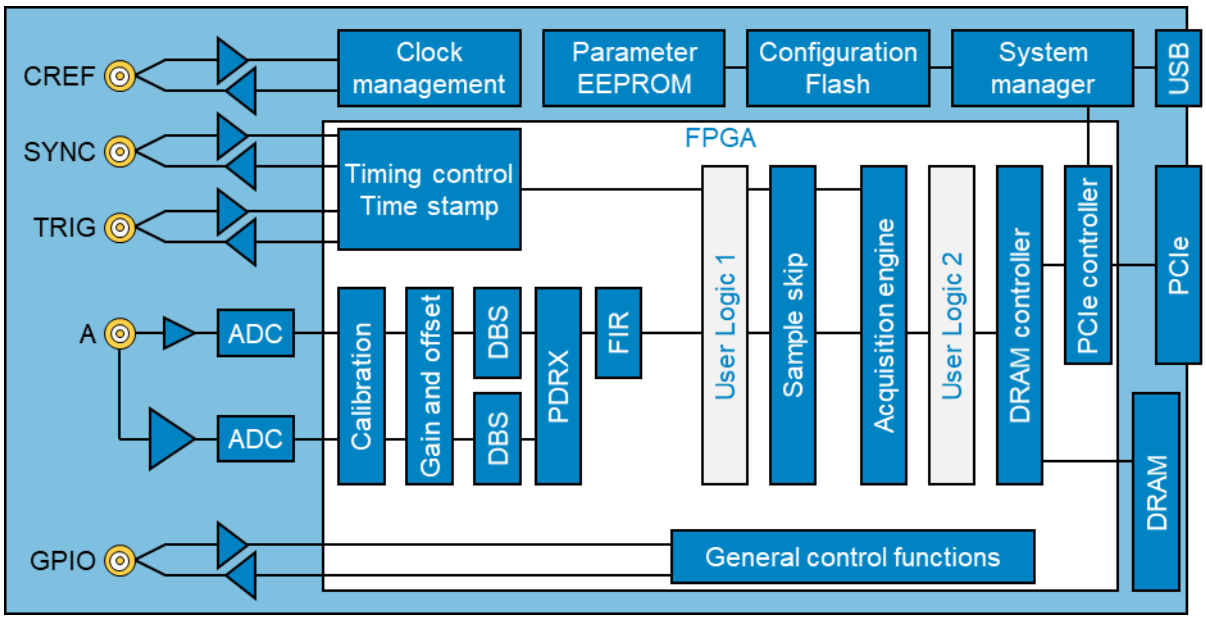

Figure 10 Block diagram ADQ35-PDRX-FWDAQ-PCIe

Figure 9 shows a block diagram of ADQ35-PDRX using FWDAQ when the channel combination is bypassed. The two signals with different gain are passed to the user for channel combination.

Figure 10 shows a block diagram of ADQ35-PDRX using FWDAQ including channel combination. There is only one output channel.

The boxes “User Logic” are available for custom real-time signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ35-PDRX-PCIe is powered from the power supply of the PC via a PCI Express 8-pin (2x4) auxiliary power supply connector. The connection in the cable should be as in Figure 11. It is also possible to operate the board from a PCI Express 6-pin (2x3) auxiliary power supply connector. Consider the power ratings for the respective connectors from the PC manufacturer.

It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.

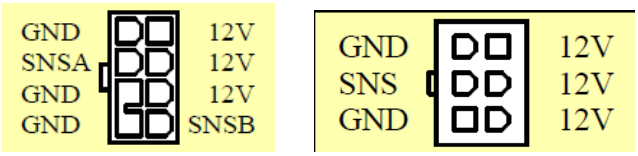

Figure 11 Power supply connection options. PCB connector.

10 GPIO EXPANSION

The FFC/FPC connector allows direct access to the FPGA for building custom expansion boards. The FFC connector requires custom firmware and is accessible through the FPGA development kit. The ADQ35-PDRX user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

11 MECHANICAL DRAWING

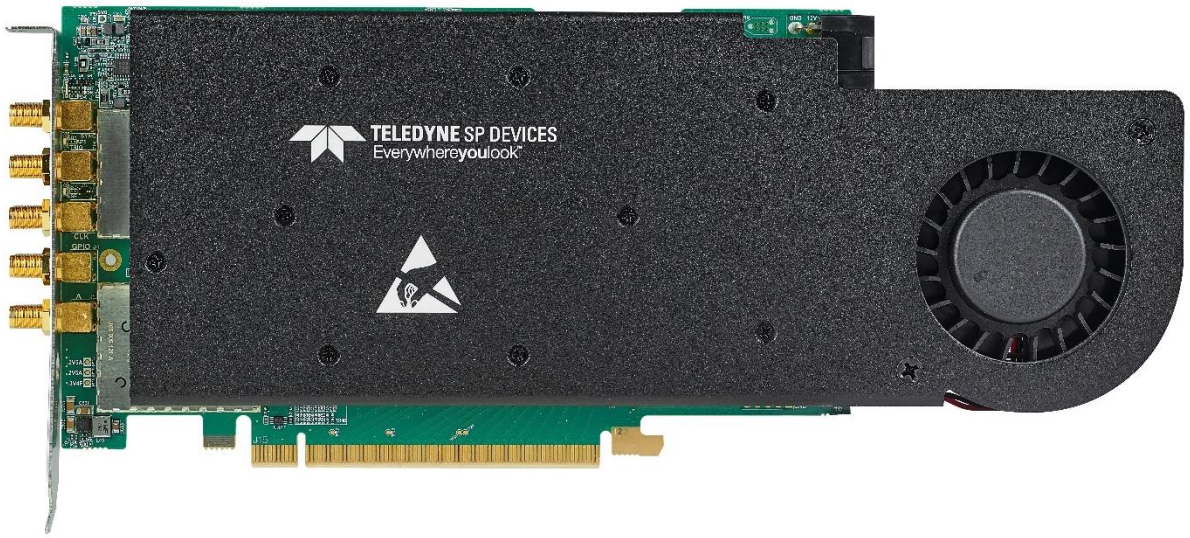

Figure 12 Photo of ADQ35-PDRX.

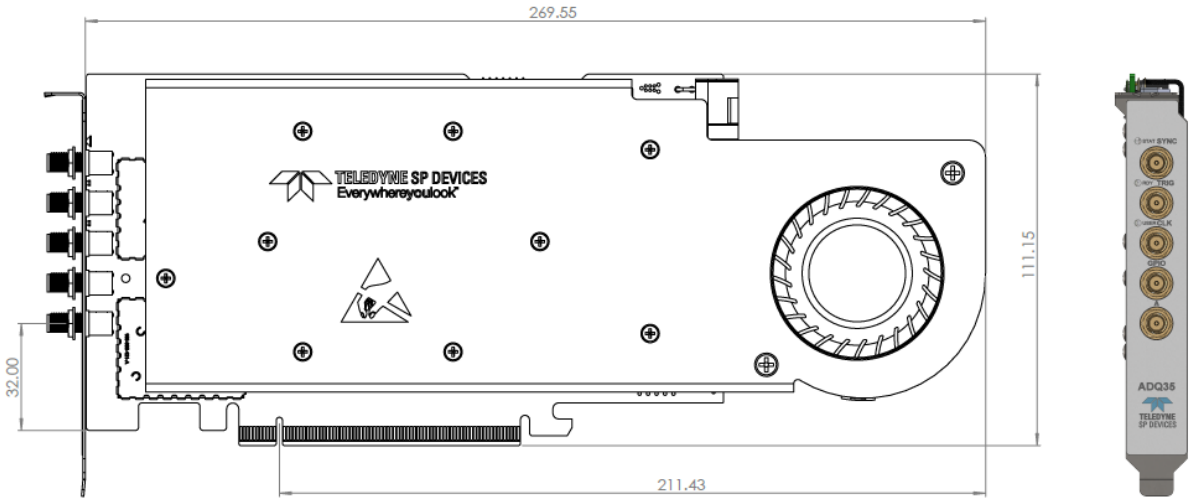

Figure 13 Mechanical drawing, dimensions in millimeters.

12 REFERENCES

Refer to Teledyne SP Devices' web site spdevices.com for the latest version of supplementary documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

20-2507 ADQ3 series development kit user guide

20-2509 ADQ35-WB datasheet

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

22-2918 ADQ35 datasheet

23-3028 ADQ3 FWPD datasheet

Important Information

Teledyne Signal Processing Devices Sweden AB (Teledyne SP Devices) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Teledyne SP Devices' general terms and conditions supplied at the time of order acknowledgment. Teledyne SP Devices warrants that each product will be free of defects in materials and workmanship, and conform to specifications set forth in published data sheets, for a period of three (3) years. The warranty commences on the date the product is shipped by Teledyne SP Devices. Teledyne SP Devices' sole liability and responsibility under this warranty is to repair or replace any product which is returned to it by Buyer and which Teledyne SP Devices determines does not conform to the warranty. Product returned to Teledyne SP Devices for warranty service will be shipped to Teledyne SP Devices at Buyer's expense and will be returned to Buyer at Teledyne SP Devices' expense. Teledyne SP Devices will have no obligation under this warranty for any products which (i) has been improperly installed; (ii) has been used other than as recommended in Teledyne SP Devices' installation or operation instructions or specifications; or (iii) has been repaired, altered or modified by entities other than Teledyne SP Devices. The warranty of replacement products shall terminate with the warranty of the product. Buyer shall not return any products for any reason without the prior written authorization of Teledyne SP Devices.

In no event shall Teledyne SP Devices be liable for any damages arising out of or related to this document or the information contained in it.

TELEDYNE SP DEVICES' EXPRESS WARRANTY TO BUYER CONSTITUTES TELEDYNE SP DEVICES' SOLE LIABILITY AND THE BUYER'S SOLE REMEDY WITH RESPECT TO THE PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES, LIABILITIES AND REMEDIES. EXCEPT AS THUS PROVIDED, TELEDYNE SP DEVICES DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT.

TELEDYNE SP DEVICES DOES NOT INDEMNIFY, NOR HOLD THE BUYER HARMLESS, AGAINST ANY LIABILITIES, LOSSES, DAMAGES AND EXPENSES (INCLUDING ATTORNEY'S FEES) RELATING TO ANY CLAIMS WHATSOEVER. IN NO EVENT SHALL TELEDYNE SP DEVICES BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFIT, LOST DATA AND THE LIKE, DUE TO ANY CAUSE WHATSOEVER. NO SUIT OR ACTION SHALL BE BROUGHT AGAINST TELEDYNE SP DEVICES MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS ACCRUED. IN NO EVENT SHALL THE ACCRUED TOTAL LIABILITY OF TELEDYNE SP DEVICES FROM ANY LAWSUIT, CLAIM, WARRANTY OR INDEMNITY EXCEED THE AGGREGATE SUM PAID TO SP BY BUYER UNDER THE ORDER THAT GIVES RISE TO SUCH LAWSUIT, CLAIM, WARRANTY OR INDEMNITY.

Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 8D
SE-583 30 Linköping
Sweden
Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com